Q.P. Code: 16EC402 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year I Semester Supplementary Examinations Feb-2021

SWITCHING THEORY AND LOGIC DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent.	6M
	b	Simplify the following Boolean expression: F = (A+B)(A'+C)(B+C).	6M

OR

2	a	Simplify the following Boolean expressions to minimum no. of literals F=(BC'+A'D)(AB'+CD')	6M
	b	State Duality theorem. List Boolean laws and their Duals.	6M

UNIT-II

3	a	Simplify the following Boolean expressions using K-map F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z Implement using NAND gates.	6M
	b	Implement the following Boolean function using NOR gates. Y=(AB'+A'B)(C+D').	6M

OR

4	a	Minimize the given Boolean function Y(A,B,C,D) = Σ(1,3,5,8,9,11,15)) using tabulation method and implement using basic gates.	6M
	b	i) Write the advantages of Tabulation method over K-Map method. ii) Write the given Boolean expression f = A+B in Sum of minterms. iii) SOP of F(x, y, z)=Σ(2, 3, 6, 7).	6M

UNIT-III

5	a	Design & implement a 4 bit binary-to-BCD code converter.	6M
	b	Design & implement Full Adder using Two Half adder and OR gate.	6M

OR

6	a	Implement the following Boolean function using 8:1 multiplexer F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D	6M
	b	Implement 2-bit Magnitude Comparator and write down its design procedure.	6M

UNIT-IV

7	a	Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop.	6M
	b	Implement 6-bit ring counter using suitable shift register. Briefly describe its operation.	6M

OR

8	a	Draw the circuit of Master Slave JK flip flop using NAND gates and explain its operation.	6M
	b	Design T Flip Flop by using JK Flip Flop and draw the timing diagram.	6M

UNIT-V

9	a	Implement the following Boolean function usingPLA F1= Σm(0,1,2,3,8,10,12,14) F2 = Σm(0,1,2,3,4,6,8,10,12,14	6M
	b	Explain the minimization procedure for determining the set of equivalent state of a specified machine M.	6M

OR

10	a	Given the 8-bit data word 01011011, generate the 12-bit composite word for the hamming code that corrects and detects single errors.	6M
	b	Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure.	6M

*** END ***